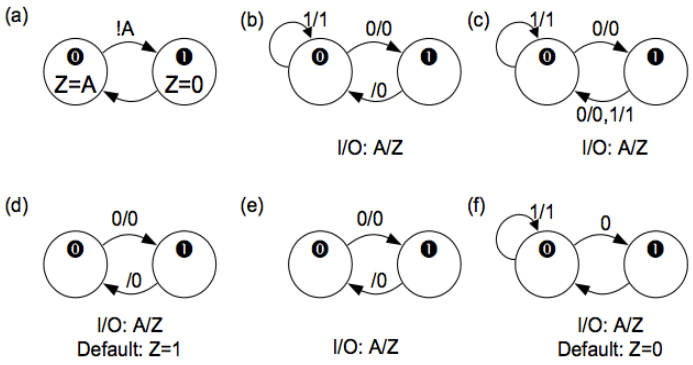
ELEC50001 EE2 Circuits and Systems

Problem Sheet 6

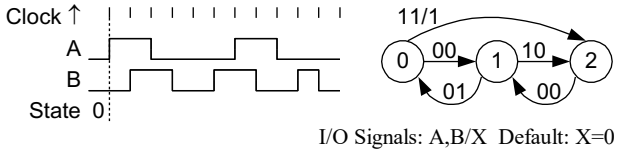
(Finite State Machines – *Lecture 9)*

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. Say which of the following state diagrams denote the same state machine as version (a). Where an arrow is marked 0/1, for example, it means when A=0, the output Z will be 1 and the transition will be taken at the next CLOCK rising edge.



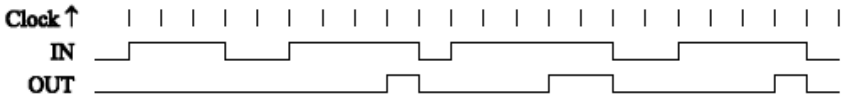
2C. The state diagram and input waveforms of a state machine are shown below. All input and state transitions occur shortly after the clock rising edge. Complete the timing diagram by indicating the value of the state during each clock cycle and by drawing the waveform of X. The initial state is 0 as shown.



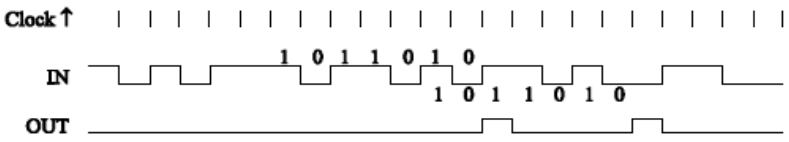
I/O Signals: A,B/X Default: X=0

3B. A synchronous state machine has its state represented by the 2-bit number S1:0 and has a single input signal DIR. The current state is stored in a D-type register whose input NS1:0 is defined by: $NS1 = S0 \oplus DIR$ and $NS0 = \overline{S1 \oplus DIR}$. Draw the state diagram for the state machine.

4C. Draw the state diagram for a state machine whose output goes high when the input is high for four or more clock cycles. As shown in the timing diagram, the output should go high during the fourth clock cycle and remain high so long as the input does. Input and state transitions occur shortly after the clock rising edge.

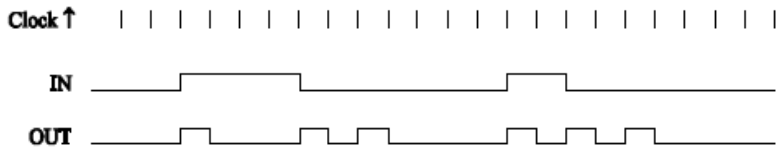


5D. Draw the state diagram for a state machine whose output goes high during the clock cycle following the reception of the input sequence 1011010. The trigger sequences can overlap as in the example below. Indicate the sequence of states followed by your design for the input sequence given below.

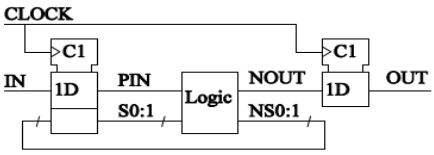


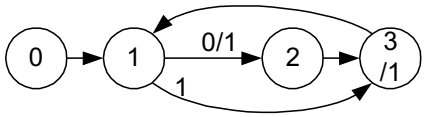
6C. A counter is required that follows the sequence 1, 2, 3, 1, 2, 3, …. Design a state machine to follow this sequence using D-type flipflops and as few gates as possible. You should ensure that the counter will reach the desired sequence regardless of its initial state.

7C. Construct the state diagram for a state machine that emits a single pulse on each rising edge of its input and a double pulse on each falling edge as shown below. Each output pulse should last exactly one clock cycle. Assume that the input signal has been synchronized with the clock rising edge. How does your design react to an input signal that goes low for less than four clock cycles?

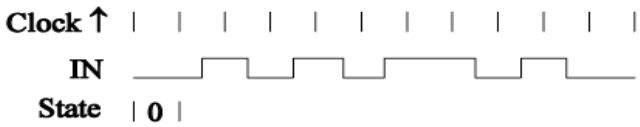


8C. In the state machine illustrated below, the contents of the logic block are defined by: $NS1 = S1 \oplus S0$, $NS0 = PIN + S1 + \overline{S0}$, $NOUT = \overline{PIN} \cdot S0 + S1 \cdot S0$ which gives the state diagram shown. Transitions of the input signal IN occur on the *falling* edge of the clock. Complete the timing diagram by indicating the sequence of states and the signals PIN, NOUT and OUT.





I/O Signals: PIN/POUT
Default: NOUT=0



9B. Implement the FSM in Question 8 in Verilog HDL.

10D. Design a finite state machine "onehot" to do the following:

when input **trigger** goes from high to low, a pulse is produce on the output **pulse_out** lasting for **width** cycles of the clock signal **sysclk**. Implement this circuit in Verilog whose interface is given below. Assume that **width** is a 10 bit number.

```
module oneshot (
sysclk,     // Clock input to the design
trigger,    // Initial the delay time_out signal
width,      // width of pulse in sysclk cycles
pulse_out   // time_out goes high for one cycle, n clock cycles after trigger goes high
);          //    End of port list
```